2 T837 Circuit Operation

This section provides a basic description of the circuit operation of the T837 paging exciter.

Note: Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 2.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts list and diagrams for the VCO PCB are in Part E.

The following topics are covered in this section.

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2.1 Introduction

The individual circuit blocks which make up the T837 are:

- synthesiser
- VCO
- paging modulator
- drive amplifier
- voltage regulators.

Each of these circuit blocks is set in its own shielded compartment, formed as an integral part of the main chassis.

The configuration of the circuit blocks may be seen on a functional level in Figure 2.1. Refer to the circuit diagrams in Section 6.2 for more detail.

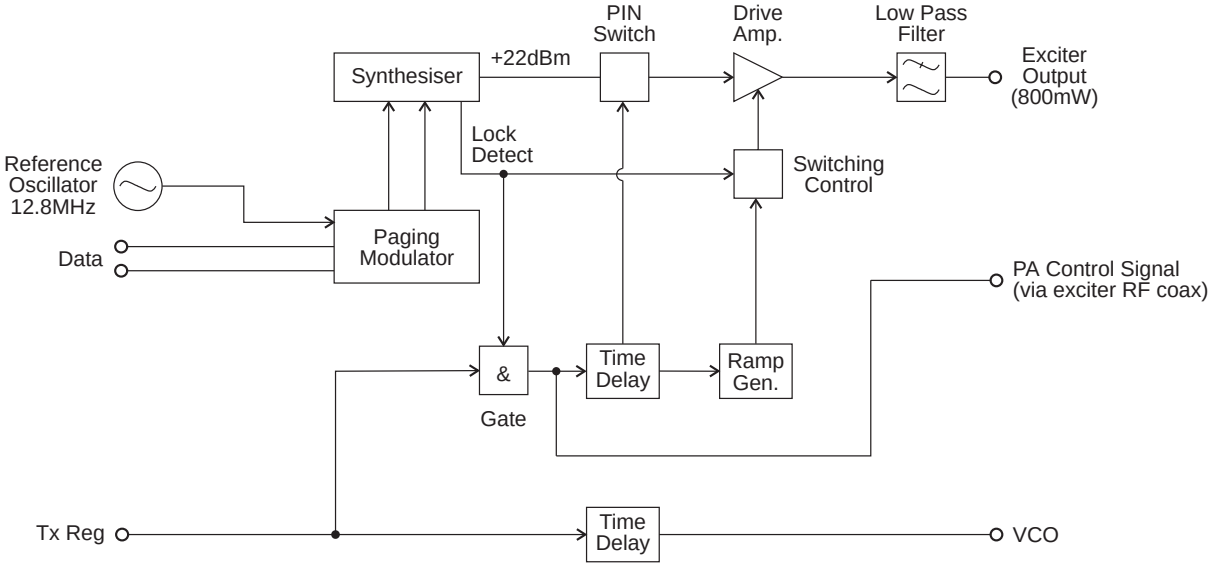

Figure 2.1 T837 High Level Block Diagram

2.2 Microcontroller

(Refer to the microcontroller circuit diagram (sheet 8) in Section 6.2.)

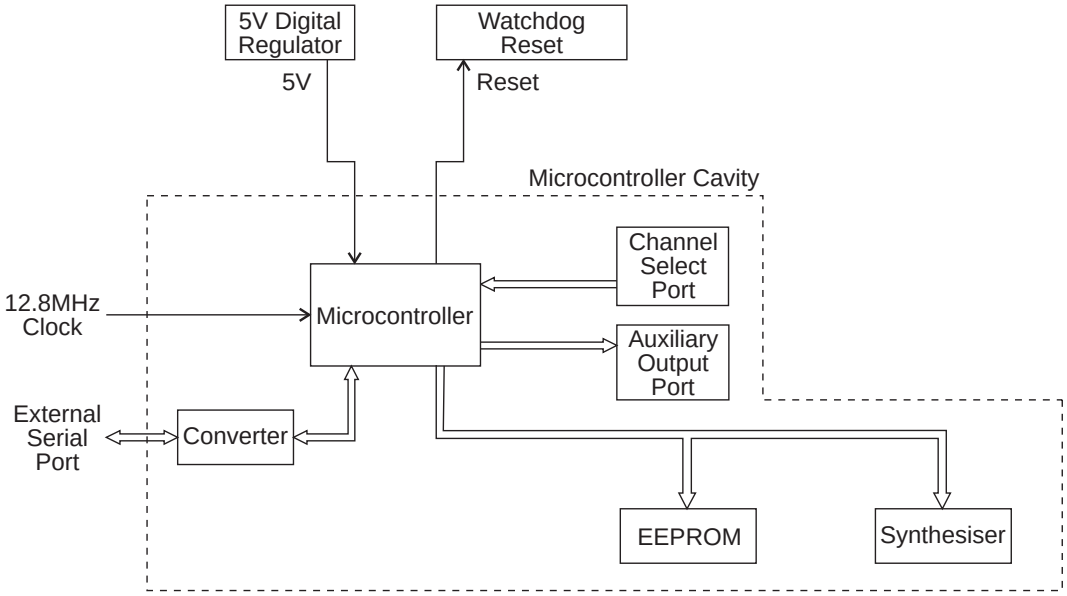

Figure 2.2 T837 Microcontroller Block Diagram

Overall system control of the T837 is accomplished by the use of a member of the 80C51 family of microcontrollers (IC810). It runs from internal ROM and RAM, thus leaving all four ports free for input/output functions.

Non-volatile data storage is achieved by serial communication with a 16kBit EEPROM (IC820). This serial bus is also used by the microcontroller to program the synthesiser (IC740).

The main tasks of the microcontroller are as follows:

- program the synthesiser;
- interface with the PGM800Win programming software at 9600 baud via the serial communication lines on D-range 1 (PL100);
- coordinate and implement timing control of the exciter;
- control the front panel "Supply" LED (refer to Section 5.3).

2.3 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram (sheet 7) in Section 6.2 and the VCO circuit diagram in Part E.)

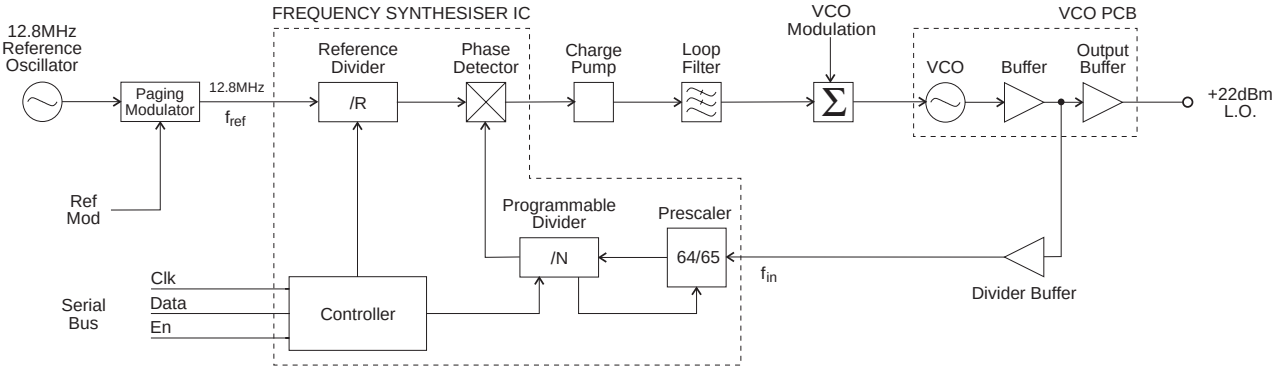

Figure 2.3 T837 Synthesiser Block Diagram

The synthesiser (IC740) employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a given reference frequency. The synthesiser receives the divider information from the control microprocessor via a 3 wire serial bus (clock, data, enable). When the data has been latched in, the synthesiser processes the incoming signals from the VCO buffer (f_{in}) and the phase modulator (f_{ref}).

A 12.8MHz reference frequency is fed from the paging modulator section to the frequency synthesiser Ref_{in} (IC740 pin 20). This reference frequency is derived from the VCXO (X101), which is locked to the internal frequency standard provided by the TCXO (X100). The reference frequency has been modulated in the VCXO by the incoming data to allow the synthesiser loop to modulate down to DC. This 12.8MHz reference frequency is divided down to 6.25kHz or 5.0kHz in the synthesiser IC (IC740).

A buffered output of the VCO (Q795) is divided with a prescaler and programmable divider which is incorporated into the synthesiser chip (IC740). This signal is compared with the phase modulated reference signal at the phase detector (also part of the synthesiser chip). The phase detector outputs drive a balanced charge pump circuit (Q760, Q770, Q775, Q780, Q785) and active loop filter (IC750 pins 5, 6 & 7) which produces a DC voltage between 0V and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and other spurious signals. Note that the VCO frequency increases with increasing control voltage.

If the synthesiser loop loses lock, a pulsed signal appears at LD (pin 2) of IC740. This signal is filtered and buffered by IC750 pins 1, 2 & 3, producing the Lock-Detect signal used to shut off the power supply to the drive amplifier. IC750 pin 1 is at 20V when the synthesiser is out of lock.

2.3.1 Two Point Modulation

Frequency modulation occurs by modulating both the VCO input and the synthesiser reference input. This process is called two point modulation and ensures a flat modulation response from 0 to 2400bps.

The PLL has a fast response time, allowing a Tx key-up time of <30ms. Because of this fast response time the PLL sees lower modulation frequencies superimposed on the VCO as an error and corrects for it, resulting in no modulation on the carrier. At modulation frequencies greater than 300Hz the loop cannot correct fast enough and modulation is seen on the carrier.

To achieve low frequency modulation, the reference oscillator is also modulated so that the phase detector of IC740 detects no frequency error under modulation. Thus, the synthesiser loop will not attempt to correct for modulation and the data frequency response of the transmitter remains unaffected.

2.4 VCO

(Refer to the VCO circuit diagram in Part E.)

The VCO transistor (Q1) operates in a common source configuration, with an LC tank circuit coupled between its gate and drain to provide the feedback necessary for oscillation. The VCO control voltage from the loop filter (IC750 pin 7) is applied to the varicaps (D1-D4) to facilitate tuning within an 8MHz band of frequencies. A trimcap (CV1) is used for coarse tuning of the VCO. The output from the oscillator circuit drives a cascode amplifier stage (Q2, Q3) which supplies +10dBm (typically) to a further stage of amplification, Q5. This is the final amplifier on the VCO PCB, and delivers +22dBm (typically) to the exciter drive amplifier.

A low level "sniff" is taken from the output of Q3 and used to drive the divider buffer (Q795) for the synthesiser (IC740).

The VCO operates at the actual output frequency of the exciter, i.e. there are no multiplier stages. The VCO is modulated by superimposing the data signal onto the control voltage and by frequency modulating the reference signal.

2.4.1 VCO Supply

The VCO is supplied from two switched +9V supplies under the control of the Tx-Reg. supply.

The VCO (Q1) and buffer amplifier (Q2 & Q3) are supplied from one +9V switched supply by Q540 via the capacitor multiplier (Q550, C550).

The output amplifier is supplied from the other +9V supply by Q520, Q530, and Q510.

A delay circuit holds the VCO on for a short time after the Tx-Reg. supply has been switched off. This is to allow the RF power circuits (both exciter and PA) to ramp down in the correct manner before the VCO is switched off.

2.5 Low Speed Paging Modulator

(Refer to the low speed paging modulator circuit diagram (sheet 2) in Section 6.2.)

2.5.1 General

The T837-2X-102X is a dedicated paging exciter. The low speed paging modulator section of the exciter accepts TTL data at the D-range input and modulates the synthesiser using a two point modulation method that provides modulation of data input frequencies of 2400bps down to DC (all 1's or all 0's).

The paging modulator section incorporates a TCXO frequency reference and a modulatable VCXO which is locked to the reference frequency from the TCXO.

The paging modulator also has provision for fitting an optional FFSK modem PCB.

2.5.2 AFC/PLL Operation

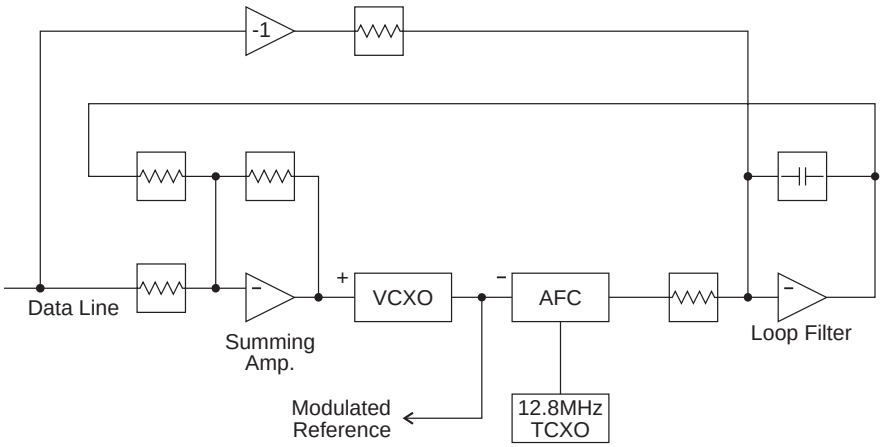

Figure 2.4 T837 AFC Block Diagram

The TCXO is the default frequency standard. In PLL mode, the slave 12.8MHz VCXO is phase locked to the TCXO. Both the TCXO and the VCXO outputs are clipped in IC100 and IC102 and then frequency divided by 4 in the twisted ring counters, IC105 (TCXO) and IC110 (VCXO). The slave VCXO is also fed to the synthesiser reference input.

Each twisted ring counter provides four divide-by-four outputs, the Q and not Q having the relative phases 0°, 90°, 180° and 270°. These two signals are combined in the two XOR gate phase discriminators in IC115 to provide two beat frequencies that are in phase quadrature. Both these outputs are filtered to pass the low frequency beat signal, which is a 5Vpp triangle wave.

The output from pin 8 of IC115 is then differentiated to provide a further 90° phase shifted square wave output on pin 14 of IC120. The amplitude of the output is proportional to the frequency difference between the TXCO and the VCXO. The square wave is then rectified by gating the signal with an inverted version of itself through a CMOS

switch. The switch is controlled by a square wave derived from the triangle wave on pin 7 of IC120. This square wave will either be in-phase or inverted with respect to the output on pin 14 of IC120, depending on whether the VCXO frequency is higher or lower than the TCXO frequency.

The output from the CMOS switch (pin 14 of IC150) is a direct voltage which has amplitude and sense that is relative to the beat frequency. This signal is used as the control voltage for the VCXO. The rectified signal is then summed with an inverted version of the data, which cancels the effect of the data on the loop filter but still allows the VCXO to follow the TCXO frequency. Although the VCXO and TCXO are not on the same frequency when data is being applied, the VCXO frequency will not drift with respect to the TCXO.

2.5.3 Data Path

The input data enters the radio via pin 12 of D-range 1 (PL100). The data is fed into the paging modulator at I/O pad P101, which is buffered by Q100, and then through an XOR gate (IC115 pins 2 & 3) which gives the option of inverting the data.

IC140 pins 5 & 6 translate the level of the signal to 9Vpp, and then the data passes through an attenuator and data filter. The data path is switched at the output of the filter by IC150 pins 1, 2 & 15, which allows the data to be removed from the AFC loop for testing purposes.

From the switch the data travels three paths:

- The first path is via RV100 to the LOOP-MOD output to modulate the VCO.
- The second path is through RV101 to the summing amp. This data modulates the control line of the VCXO, which produces the modulated reference.
- The third data path, which originates at the switch, is the feedforward data path. The data is inverted, attenuated by RV102 and then summed with the output of the AFC. The effect of this data path is to stop the loop filter from correcting the VCXO frequency deviation caused by the data on the data line.

2.5.4 External Reference Frequency (T837-2X-1021 Only)

The paging modulator section of the T837-2X-1021 exciter incorporates an additional synthesiser (*IC200) which can be configured to provide a 12.8MHz reference frequency from an external frequency standard. This external frequency can be from 100kHz up to 25.6MHz in 100kHz steps.

When using an external reference, you must set the onboard synthesiser's reference frequency according to the frequency of the external reference. This is achieved by placing resistors *%R240 - *%R247 in a pattern corresponding to a binary number which represents the reference divider ratio (see Section 3.6).

The internal TCXO (%X100) is used as the standard reference frequency, but is phase-locked to the external frequency when this is applied.

When there is no external reference frequency present, *Q104 is turned off and *IC160 switches 2.5V DC to the AFC input of the internal TCXO. The reference frequency can be adjusted by the trimmer on the TCXO itself.

When an external reference frequency is present, *Q104 switches on and *IC160 switches the synthesiser phase detector output voltage to the AFC input of the internal TCXO. A buffered 12.8MHz output of the internal TCXO is fed back to the synthesiser oscillator input and compared with the external reference frequency, thus ensuring that the internal TCXO is phase-locked to the external reference frequency.

The synthesiser Lock-Detect signal drives an LED *D116 on the main PCB which is lit when the synthesiser is locked to the external reference frequency. The Lock-Detect signal is also fed to pin 8 of D-range 1 (PL100) for external monitoring purposes. The output is low when the synthesiser is locked.

2.5.5 Keying Inputs

There are two ways to key the exciter:

- pulling the Tx-Key line low (pin 13 on D-range 1 [PL100]) at the rear of the set);
- via the modem carrier detect line when the optional modem PCB is fitted.

Note: Link S100 must be connected when using the Tx-Key line input.

2.5.6 Paging Modulator Links

Three solder links are provided in the paging modulator circuit. Their functions are described in the following table:

Link	Function	Standard Setting	Description
S100	Tx-Key	linked	ties the Tx-Key line to +5V for earthed Tx-Key line operation
S101	invert data	not linked	inverts the incoming data
S102	invert key	not linked	inverts the key line (connected when using modem carrier detect)

2.6 Power Supply & Regulator Circuits

(Refer to the regulators circuit diagram (sheet 6) in Section 6.2.)

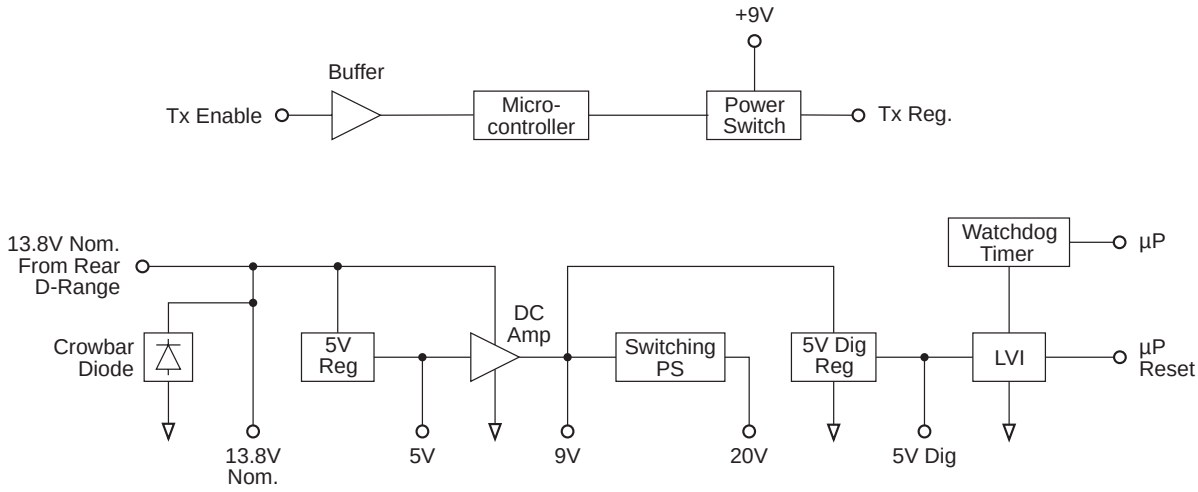

Figure 2.5 T837 Power Supply & Regulators Block Diagram

The T837 is designed to operate from a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC630) runs directly from the 13.8V rail, driving much of the synthesiser circuitry. It is also used as the reference for a DC amplifier (IC640, Q630, Q620) which provides a medium current capability 9V supply.

A switching power supply (Q660, Q670) runs from the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC750), giving a VCO control voltage range of up to 20V, and the Lock-Detect amplifiers.

Ultimate control of the transmitter is via the Tx-Reg. supply, switched from 9V by Q610. This is enabled via the Tx-Enable signal from the modulator, and microprocessor.

A crowbar diode is fitted for protection against connection to a power supply of incorrect polarity. It also provides transient overvoltage protection.

Note: A fuse must be fitted in the power supply line for the diode to provide effective protection.

2.7 Transmit Timers

The transmit tail timer, transmit timeout timer and transmit lockout timer can all be set from PGM800Win. The fields for setting these are found on the system information page. These three timers operate as follows (refer also to Figure 2.6):

Timer	Function	Adjustment
Transmit Tail	Sets the tail time during which the transmitter stays keyed after the external key source has been removed.	0-5 seconds in 100ms steps[a]
Transmit Timeout	Sets the maximum continuous transmission time. Once the timer has timed out, the transmitter must be keyed again, unless prevented by the transmit lockout timer.	0-300 seconds[b] in 10 second steps
Transmit Lockout	Sets the period of time that must elapse after a timeout before the transmitter can re-transmit. Once the timer has timed out, the transmitter can be keyed again.	0-60 seconds in 10 second steps

a. Adjustable in 20ms steps in PGM800Win version 2.12 and later.
b. Adjustable from 0 to 600 seconds in PGM800Win version 2.12 and later.

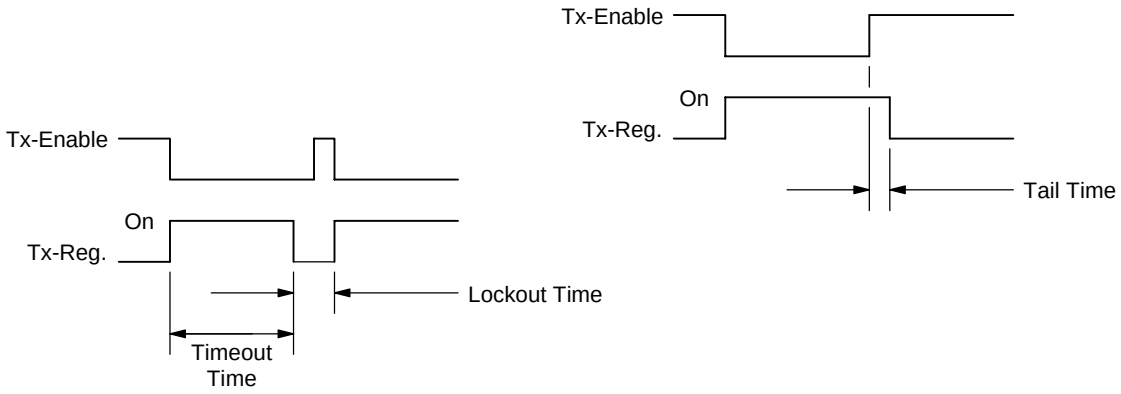

Figure 2.6 T837 Transmit Timers

2.8 Exciter Drive Amplifier

(Refer to Figure 2.1 and the exciter circuit diagram (sheet 3) in Section 6.2.)

A two-stage, wide band amplifier (Q365, Q370) provides an output level of approximately 800mW (+29dBm) for an input of 170mW (+22dBm) from the VCO. IC330 pins 5, 6 & 7, Q310, and Q315 provide a 10.5V regulated supply for the exciter.

To reduce the spurious output level when the synthesiser is out-of-lock, the Tx-Reg. and Lock-Detect signals are gated to inhibit the exciter control circuit and to switch off the RF signal at the input to the drive amplifier. This is achieved by a PIN switch attenuator (D340, D350, D360).

Cyclic keying control is provided by additional circuitry consisting of several time delay, ramp and gate stages:

- Q305, IC330 pins 5, 6 & 7 power ramping
- Q340, Q345 Tx-Reg. and $\overline{\text{Lock-Detect}}$ gate
- Q320, Q325, Q330, Q335 delay and PIN switch drive.

This is to allow the RF power circuits (both exciter and PA) to ramp up and down in a controlled manner so that minimal adjacent channel interference is generated during the transition.

R359, R342 and R344 form a 6dB attenuator to provide good VCO/drive amplifier isolation.

The output attenuator (R360, R362, R364, R366) assists in reducing exciter/PA interaction while also ensuring a good match for Q370.

Note: The exciter provides a DC control signal to the PA via the RF coax. This is injected via L390.

